Curriculum for M.Tech

Electronics & Communication Engineering with Specialization in Microelectronics and VLSI Systems

From The Academic Year 2025

(Approved in Senate 61)

Indian Institute of Information Technology Design and Manufacturing, Kancheepuram

Chennai-600 127

Semester 1					
Category	**Course Name**	**L**	**T**	**P**	**C**
PCC	MOS Modeling for VLSI Circuits	3	1	0	4
PCC	VLSI System Design	3	1	0	4
PCC	VLSI Testing and Testable Design	2	0	4	4
PCC	Device Modeling and Simulation Practice	0	1	2	2
PEC	Programme Elective Course 1	3	1	0	4
PEC	Programme Elective Course 2	3	1	0	4
					22
Semester 2					
Category	**Course Name**	**L**	**T**	**P**	**C**
PCC	CMOS Analog VLSI Design	3	1	0	4
PCC	High Level Verification with UVM	2	0	4	4
PCC	IC Fabrication	2	0	4	4
PCC	CMOS VLSI Design Practice	0	0	4	2
PEC	Programme Elective Course 3	3	1	0	4
PEC	Programme Elective Course 4	3	1	0	4
					22
Summer					
PCD	M Tech Dissertation (MTD) Phase I	0	0	8	4
					4
Semester 3					
Category	**Course Name**	**L**	**T**	**P**	**C**
PCD	M Tech Dissertation (MTD) Phase II	0	0	24	12
					12
Semester 4					
Category	**Course Name**	**L**	**T**	**P**	**C**
PCD	M Tech Dissertation (MTD) Phase III	0	0	28	14
					14
	TOTAL CREDITS				**74**

Semester wise Credit Distribution	**Credits**						
Category	**S1**	**S2**	**Summer**	**S3**	**S4**	**Total**	**%**
Program Core Course (PCC)	14	14	0	0	0	28	37.8
Program Elective Course (PEC)	8	8	0	0	0	16	21.6
Professional Career Development (PCD)	0	0	4	12	14	30	40.5
Total	22	22	4	12	14	74	100
Cumulative Credits	**22**	**44**	**48**	**60**	**74**	**74**	

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COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">MOS Modeling for VLSI Circuits</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">Electronics and Communication Engineering</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>3</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td rowspan="2">To be offered for</td><td rowspan="2">CORE:
M.TECH MVS</td><td>Type</td><td colspan="2">Core ▬</td><td colspan="2">Elective ☐</td></tr>
<tr><td>Status</td><td colspan="2">New ☐</td><td colspan="2">Modification ▬</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="2">Submitted for approval</td><td colspan="3">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To demonstrate and apply basic concepts of semiconductor physics relevant to devices
• To describe and use physics-based numerical and analytical device modelling for the inclusion in circuit applications</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">At the end of the course, the students would be able to
• Model any kind of MOS Devices in 2-D or 3-D
• Relate the models for further inclusion in circuits</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">Semiconductors: Energy bands; Thermal equilibrium carrier concentration. Excess carriers, quasi-Fermi levels; Recombination of carriers, lifetime. Carrier transport by drift, mobility; Carrier transport by diffusion; Continuity equation. Diffusion length. (8 L + 3 T)
Quantitative theory of PN junctions: Steady state I-V characteristics under forward bias, reverse bias, and illumination. Capacitances. Dynamic behavior under small and large signals. Breakdown mechanisms. (6 L + 2 T)
Theory of Field Effect Transistors: Analysis of MOS capacitor. Calculation of threshold voltage. Static I-V characteristics of MOSFETs and their models. (6 L + 2 T)
Long-Channel MOS Transistor, Introduction All-Region Models, Strong Inversion Models, Weak Inversion Models, Effective Mobility. (7 L + 3 T)
Small-Dimension Effects - Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain-Induced Barrier Lowering, Hot Carrier Effects, Velocity Overshoot Ballistic Operation, Polysilicon Depletion. (8 L + 2 T)
Small-Dimension Effects-Modelling for Circuits Simulation- Quantum-Mechanical Effects; Gate Current, Junction Leakage, Scaling and New Technologies, Approaches, and Properties of Good Models, Model Formulation Considerations (7 L + 2 T)</td></tr>
<tr><td>Text Books</td><td colspan="6">1. Nandita Dasgupta, Amitava Dasgupta, “Semiconductor Devices: Modelling and Technology”, Prentice Hall, 2004. ISBN: 9788120323988.
2. Y. Tsividis and C. McAndrew, Operation and Modeling of the MOS Transitor, Oxford University Press, 2011. ISBN: 0195170156</td></tr>
<tr><td>Reference Books</td><td colspan="6">1. BSIM Manuals available on BSIM homepage on the internet.
2. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2013. ISBN: 1107635713</td></tr>
</table>

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COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">VLSI System design</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>3</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td rowspan="2">To be offered for</td><td rowspan="2">M.TECH MVS</td><td>Type</td><td colspan="2">Core ☐</td><td colspan="2">Elective ☐</td></tr>
<tr><td>Status</td><td colspan="2">New ☐</td><td colspan="2">Modification ☐</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="2">Submitted for approval</td><td colspan="3">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To provide an in-depth understanding of digital CMOS system design from register-transfer level (RTL) to gate-level implementation.
• To develop expertise in hardware modelling using HDLs for control and datapath-intensive designs.
• To introduce static timing analysis, design optimization, low-power techniques, and integration considerations in complex VLSI systems.
• To equip students with the knowledge to architect, analyze, and optimize performance-constrained and area-efficient digital designs.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">By the end of the course, students will be able to:
1. Analyze and model complex digital systems at the RTL using Verilog/VHDL.
2. Evaluate performance metrics (timing, power, area) of digital designs and apply design techniques such as pipelining, retiming, and FSM optimization for high-performance systems.
3. Describe the RTL-to-GDSII flow, synthesis constraints, floorplanning, and clocking strategies.
4. Propose low-power strategies such as clock gating and supply scaling at the system level.
5. Analyze impact of interconnect and parasitics in submicron designs using academic models.</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">CMOS Logic Gate Design: Review of CMOS inverter, Gates, sizing, delay, logical effort (6L + 2T)
Sequential Logic Design: Latches and flip-flops, clocking schemes, metastability (6L + 1T)
Interconnect Modelling: RC delay, Elmore delay, wire sizing and buffer insertion (4L + 1T)
FSMs and RTL Design: FSM modelling styles, one-hot and binary encoding, RTL principles (3L + 1T)
Hierarchical Design Methodologies: Pipelining and parallelism, Top-down vs. bottom-up, module hierarchy, system abstraction levels (3L + 1T)
HDL Modelling: Basics Verilog/VHDL syntax, modules, data types, combinational logic modelling (3L + 1T)
HDL Modelling: Sequential Circuits, Sequential blocks, FSMs, test benches and simulation strategies (3L + 1T)
RTL to Gate-Level Synthesis: Behavioural vs. structural synthesis, constraints, optimization concepts (3L + 1T)
Timing Analysis Concepts: Setup/hold violations, timing arcs, clock skew and jitter basics (3L + 1T)
Static Timing Analysis (STA): Delay models, arrival/required times, slack analysis, timing reports (3L + 1T)</td></tr>
</table>

	Low Power Design Techniques: Sources of power, switching activity, clock gating, voltage scaling (3L + 1T) **SoC Design Concepts:** System integration, IP reuse, NoC intro, AMBA/AXI overview (conceptual only) (2L)
Text Books	3. Neil H. E. Weste & David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Pearson, 2010. ISBN-13: 978-0-321-54774-3 4. David Money Harris & Sarah L. Harris, Digital Design and Computer Architecture, 2nd ed., Morgan Kaufmann, 2012. ISBN-13: 978-0-12-394424-5
Reference Books	3. Jan M. Rabaey, Anantha Chandrakasan & Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd ed., Pearson, 2015. ISBN-13: 978-0-13-335672-0 4. Wayne Wolf, Modern VLSI Design: IP-Based Design, 4th ed., Pearson, 2008. ISBN-13: 978-0-13-714579-0 5. Keshab K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, Reprint ed., Wiley, 2010. ISBN-13: 978-0-470-17035-7

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COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">VLSI testing and testable design</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
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<tr><td>Status</td><td colspan="2">New □</td><td colspan="2">Modification ■</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• The course aims at imparting skills required for the design of an efficient testable circuit and optimal test vectors to detect all faults</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">• At the end of the course, the students would be able to Model the faults in the combination and sequential circuits
• Perform the fault analysis and test pattern generation using ATPG algorithm
• Build testable designs, generate and verify test vectors</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">Basic of Test - Design and Test, Test Goals, ATE Architecture and Instrumentation, Testing needs, Quality – HTOL, Automotive std basics, Test Requirements (required in design) & cost driven, Future Testing methodology to address upcoming design nodes (3D IC). (3L)

Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, RTL Boundary Scan and Boundary Scan Description Language. Overview of IEEE standards and IEEE P1500 & IEEE1838 IEEE 1149.1,1149.6 JTAG, RTL validation of a Spare register and understanding of JTAG FSM/IR/DR, (2L),

Design changes for testing: Additional IOs, test clock muxing, CGC logic, On chip clocking, Multisite testing and limited pin count (2L)

Fault and Defect Modeling: Fault Modeling, Structural Gate Level Faults, Issues Related to Gate Level Faults, Transition Faults, Path Delay faults, Memory Faults, Iddq, burnin test (3L)

Design for Test by Means of Scan: Making circuits Testable, Testability Insertion, Full Scan DFT Technique, Scan Architectures. (3L)

Test pattern Generation Methods and Algorithm: Test Generation Basics, Controllability and Observability, Combinational and sequential Test Generation, Static and At-speed ATPG, IDDQ (2L)

Deterministic Test Generation Algorithms: Deterministic Test Generation Methods, Sequential Circuit Test Generation, Test Data Compaction. (2L)

Logic Built-in Self-test: BIST Basics, Test Patter Generation, Output Response Analysis, BIST Architectures, RT Level BIST Design. Introduction to IOBIST (3L)

Memory Testing by Means of Memory BIST: Memory Testing, Memory Structure, Memory Repair, Redundancy, Memory Components (Sector/Bank/Array/Decoder/Sense Amp). (2L)</td></tr>
</table>

	Fault Simulation Application and Methods: Fault Simulation, Fault Simulation Applications, Fault Simulation Technologies. (2L) Test Compression: Test Data Compression, Compression Methods and Decompression Methods. (2L) Advanced topics: top level DFT, DRC, connectivity checks for DFT, Test vector generation and simulation, Test cost analysis (w.r.t Test Time), Test mode constraints, test mode timing closure, IR issues during at-speed capture, ATE debug and production testing, testing analog/mixed signal blocks (2L) Lab 1. Synthesis (4P) 2. Formal verification (4P) 3. Memory BIST insertion and verification (4P) 4. Scan Insertion (4P) 5. ATPG (4P) 6. scan verification (4P) 7. Compression and verification (4P)
Text Books	5. Michael L. Bushnell, Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, Springer, 2004. ISBN: 79237991-8 **6. VLSI Test Principles and Architectures: Design for Testability,** Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, Elseveir ISBN: 9781493300860
Reference Books	6. ZainalabedinNavabi, Test and Testable Design using HDL Models and Architecture, 1st edition, Springer, 2010, ISBN: 978-1-4419-7547-8. 7. M. Abramovici, M. A. Breuer and A. D. Figriieta, Digital Systems Testing and Testable Design, Wiley-IEEE Press, 1994, ISBN: 978-0-7803-1062-9. 8. Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, 1st edition, Cambridge University Press, 2003. ISBN: 0521-77356-3

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<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">Device Modelling and Simulation Lab</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">Electronics and Communication Engineering</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
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<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To make the students familiar with semiconductor device Physics.
• To impart a flavour of different semiconductor device modelling with the help of simulation tools.
• The lab is intended to teach students about device structure and provide confidence to design the device structure and plotting necessary characteristics in relevant device modelling tools.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">At the end of the course, students would be able to:
• Familiarize with Industry-Standard TCAD Tools
• Simulate and analyse structure, doping profile, terminal characteristics, and distributions of carriers, current, field, potential and energy band diagrams within 2-dimensional device structures</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">1. Overview of TCAD Tools (1P)
• Introduction to Technology Computer-Aided Design (TCAD) and its significance in semiconductor device modeling.
• Inputs and outputs of process and device simulations.
• Overview of common TCAD tools (e.g., Synopsys Sentaurus, Silvaco Atlas).
2. Device Simulation using SDE (Structure Editor) (2P)
• Designing 2D and 3D semiconductor structures using scripting languages.
• Implementation of analytical doping profiles.
• Strategies for meshing in 2D/3D simulations to ensure numerical accuracy and efficiency.
3. Device Simulation using SDevice (3P)
• Implementation of physics-based models for device simulation.
• Mathematical foundation of device equations (Poisson's equation, continuity equations, transport models).
• Detailed understanding of the solve section for electrical simulations.
4. Process Simulation (3P)
• Simulation of semiconductor fabrication steps.
• Observation and analysis of: Final device structure, Doping profiles across the device
5. Electrical Characterization (3P)</td></tr>
</table>

	• Extraction and analysis of I-V and C-V characteristics of a 3-Terminal MOS (3T MOS) device. • Electrical characterization techniques for Silicon-On-Insulator (SOI) MOSFETs. • Parameter Extraction, Compact Models, Benchmark Tests, Small Signal Modelling including conductance parameters.
Text Books	1. C K Maiti, "Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications", Jenny Stanford Publishing; 1st Edition, 2017, ISBN: 978-9814745512. 2. Wu, Yung-Chun, Jhan, Yi- Ruei, "3D TCAD Simulation for CMOS Nanoeletronic Devices", Springer, 2017, ISBN 978-981-10-3066-6.
Reference Books	1. C K Sarkar, "Technology Computer Aided Design: Simulation for VLSI MOSFET", CRC Press, 1st Edition, 2013, ISBN: 978-1466512658. 2. J.-P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer, 2008, ISBN: 978- 0-387-71751-7 3. TCAD Manual (Available Online)

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<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">CMOS Analog VLSI Design</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
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<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To develop a strong foundation in CMOS analog circuit design and analysis.
• To train students in designing biasing circuits, amplifiers, and operational amplifiers using CMOS technology.
• To provide analytical and practical understanding of frequency response, stability, and noise in analog circuits.
• To introduce layout strategies for precision analog design with emphasis on matching and parasitic minimization.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">By the end of the course, students will be able to:
1. Analyze MOSFET behavior in analog operation and derive small-signal models.
2. Design current mirrors, differential amplifiers, and multi-stage op-amps.
3. Evaluate gain, bandwidth, stability, and compensation techniques for analog circuits.
4. Analyze thermal and flicker noise in analog blocks and optimize for low-noise design.
5. Apply layout practices such as common-centroid structures for precision and symmetry.
6. Simulate and validate analog designs using EDA tools and interpret performance metrics.</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">MOSFET Modeling and Device Physics: MOS I-V equations, second-order effects, small-signal model, gm, ro (2L + 1T)
Biasing and Current Mirrors: Simple mirror, cascode mirror, Wilson mirror (1L + 1T)
Single-Stage Amplifiers: CS, CG, source follower, gain, impedance, Miller effect (2L + 1T)
Differential Pairs and Active Loads: Operation, differential gain, CMRR, input/output resistance (3L + 1T)
Fully Differential Amplifiers and CMFB: CMFB design, fully differential op-amps, biasing strategies (5L + 1T)
Frequency Response: Transfer function, poles/zeros, Bode plots, dominant pole approx. (3L + 1T)
Stability and Compensation: Phase/gain margin, feedback stability, Miller compensation (3L + 1T)
Op-Amp Architectures: Two-stage and telescopic op-amps, gain/swing/slew rate (7L + 2T)
Advanced Op-Amp Design: Folded cascode, gain boosting, output stages (3L + 1T)</td></tr>
</table>

	Bandgap Reference Circuits: basic bandgap idea, V_{BE}-referenced sources, constant-gm biasing, startup circuits (4L + 1T) **Noise in CMOS Circuits:** Thermal, flicker noise, input-referred noise, low-noise design (3L + 1T) **Mismatch and Layout for Analog Design:** Systematic and random mismatch, common-centroid layout, routing, guard rings (4L + 1T) **Case Studies:** Op-amp, comparator design, biasing networks, Low Dropout regulator (2L + 1T)
Text Books	1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., McGraw-Hill Education, 2016. ISBN-13: 978-0-07-252493-2; ISBN-10: 0072524934 2. Philip E. Allen & Douglas R. Holberg, CMOS Analog Circuit Design, 2nd ed., Oxford University Press, 2002. ISBN-13: 978-0-19-511644-1; ISBN-10: 0195116445
Reference Books	1. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 3rd ed., Wiley, 2019. ISBN-13: 978-1-119-45804-1 2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis & Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 6th ed., Wiley, 2019. ISBN-13: 978-1-119-82988-8 3. David A. Johns & Ken Martin, Analog Integrated Circuit Design, 1st ed., Wiley, 1997. ISBN-13: 978-0-471-33250-2

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COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">High level verification with system verilog and UVM</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>2</td><td>0</td><td>4</td><td>4</td></tr>
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<tr><td>Status</td><td colspan="2">New □</td><td colspan="2">Modification ■</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To impart in depth knowledge and hands-on on the Design, Simulation and Verification Flow of Digital Circuits & Systems. verification of complex VLSI circuits with digital building blocks.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">• At the end of the course, the students would be able to understand complex RTL designs, understand verification requirements, write testplan, build testbench in System Verilog and UVM, run simulations and debug issues</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">1. Introduction to verification: test- bench, DUT, test plan, various verification technologies, verification pan, coverage, quick review of verilog based TBs (2L+1P)

2. Basic System Verilog: SystemVerilog Overview, Standard Data Types and Literals, Procedures and Procedural Statements, Operators, User-Defined Data Types and Structures, Hierarchy and Connectivity, Static Arrays, Tasks and Functions, Interfaces, Simple Verification Features, Clocking Blocks, Random Stimulus, Generate & analyze functional coverage, code coverage, line coverage & FSM coverage (3L + 5 P)

3 Advanced system verilog: Basic Classes, Polymorphism and Virtuality, Class-Based Random Stimulus, Interfaces in Verification, Covergroup, Coverage, Queues and Dynamic and Associative Arrays (QDA), Introduction to Assertion-Based Verification (ABV), Introduction to SystemVerilog Assertions (SVA), Threads and interprocess communication (10L+8 P)

4. Universal Verification Methodology (ŪVM)

SV Interfaces and BFM, Object Oriented Programming, UVM Test bench components: Driver, Sequence, Sequencer, Monitor, Scoreboard, UVM Phases, Configurations, Reporting, TLM, Agent, Env and Test, Test Scenarios and sequences',UVM Test bench Execution with test scenarios, Register Abstraction Layer (RAL) (13L+ 14P)</td></tr>
<tr><td>Text Books</td><td colspan="6">7. Chris Spear and Greg Tumbush, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd edition, Springer. 2012: ISBN 978-1-4614-0714-0
8. UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, 2013, ISBN: 0974164933.</td></tr>
<tr><td>Reference Books</td><td colspan="6">9. SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, ISBN-13: 978-0387333991
10. Donald Thomas, Logic Design and Verification Using SystemVerilog, 2016, ISBN: 1523364025</td></tr>
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	11. Stuart Sutherland, Simon Davidmann, Peter Flake: System Verilog for design - A Guide to Using SystemVerilogor Hardware Design and Modeling, 2nd Edition, Springer, ISBN 978-1-4757-6684-4 12. Janick Bergeron: Writing Testbenches using **SystemVerilog, Sprunger, ISBN** 0-387-29221-7 13. Srikanth Vijayaraghavan & Meyyappan Ramanthan Srikanth Vijayaraghavan & Meyyappan Ramanthan, A Practical Guide for SystemVerilog Assertions, Springer, ISBN 0-387-26049-8

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COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">IC Fabrication/VLSI Technology Theory and Lab</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE/Dr. Tejendra Dixit</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>2</td><td>0</td><td>4</td><td>4</td></tr>
<tr><td rowspan="2">To be offered for</td><td rowspan="2">M.TECH MVS</td><td>Type</td><td colspan="2">Core ■</td><td colspan="2">Elective □</td></tr>
<tr><td>Status</td><td colspan="2">New □</td><td colspan="2">Modification ■</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To integrate the perspectives of Circuits and Systems on technology.
• To provide an in-depth comprehension of the design of intricate VLSI devices and synthesis techniques for manufacturing.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">At the end of the course, the students will be able to
• Recognize the complexities inherent in VLSI circuit fabrication.
• Comprehend the diverse methods required for the fabrication of VLSI devices.
• Acquire hands-on experience and knowledge of the fabrication processes for current and forthcoming generation devices.</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">Theory
• Introduction to VLSI Design, Bipolar Junction Transistor Fabrication, MOSFET Fabrication. (2L)
• Crystal Structure of Si, Defects in Crystal, Crystal growth (2L)
• Epitaxy, Vapour phase Epitaxy, Doping during Epitaxy, Molecular beam Epitaxy (4L)
• Oxidation –Kinetics, Rate constants, Dopant Redistribution, Oxide Charges (5L)
• Diffusion-Theory of Diffusion, Doping Profiles, Diffusion Systems, Ion Implantation- Process, Annealing of Damages, Masking during Implantation (4L)
• Lithography, immersion lithography, e-beam lithography (5L)
• Etching- Wet Chemical Etching, Dry Etching, Plasma Etching, Si, SiO_2, SiN and other materials (3L)
• Deposition-Plasma Deposition, Metallization, Problems in Aluminium Metal contacts, Copper interconnects (3L)
• MOSFET - Metal gate vs. Self-aligned Poly-gate, Tailoring of Device Parameters, CMOS Technology, Latch - up in CMOS, MOSFET structures with strained channels and high-k gate dielectrics, Bi-CMOS Technology (6L)
Practice:
Characterization
• Electrical: Semiconductor parameter analyser and probe station
• Thickness: Surface profilometer
• Optical: UV-visible spectrometer and Raman Characterization
• Morphology: SEM and Optical Microscope</td></tr>
</table>

	Device Type: • Si/SiO_2/Metal based MOS capacitor; Bottom gate top contact MOSFET • Si based photodetector; Si based Schottky diode • Si/SiO_2 based memristor • Si/SiO_2 based humidity sensor; Si/SiO_2 based temperature sensor • Wet and Dry oxidation of Si • Wet etching of Si and SiO_2 • CVD growth of epitaxial layers
Text Books	9. Sorab K. Ghandhi, VLSI Fabrication Principles- Silicon and Galium Arsenide, Wiley; Second edition, ISBN: 978-8126517909, 2008. 10. James D. Plummer, Peter B. Griffin, Integrated Circuit Fabrication: Science and Technology, 1st Edition, Cambridge University Press, ISBN: 978-1009303583, 2023.
Reference Books	14. S. M. Sze, VLSI Technology, McGraw-Hill Education, Second edition, ISBN: 978-0070582910, 2017. 15. J. Plummer, M. D. Deal, P. B. Griffin, Silicon VLSI Technology, Fundamentals, Practice and Modeling, Pearson Higher Education, 1st Edition, ISBN: 978-0130850379, 2000. 16. Stephen A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford Univ, Second edition, ISBN: 978-0195136050, 2001.

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY
DESIGN AND MANUFACTURING (IIITDM) KANCHEEPURAM

COURSE FORMAT

<table>
<tr><td>Course Code</td><td></td><td>Course Title</td><td colspan="4">CMOS VLSI Design Lab</td></tr>
<tr><td rowspan="2">Dept./Faculty proposing the course</td><td rowspan="2">ECE</td><td rowspan="2">Structure (LTPC)</td><td>L</td><td>T</td><td>P</td><td>C</td></tr>
<tr><td>0</td><td>0</td><td>4</td><td>2</td></tr>
<tr><td rowspan="2">To be offered for</td><td rowspan="2">M.TECH MVS</td><td>Type</td><td colspan="2">Core ■</td><td colspan="2">Elective □</td></tr>
<tr><td>Status</td><td colspan="2">New ■</td><td colspan="2">Modification □</td></tr>
<tr><td>Pre-requisite</td><td></td><td colspan="3">Submitted for approval</td><td colspan="2">Senate 62</td></tr>
<tr><td>Learning Objectives</td><td colspan="6">• To provide hands-on experience in analog and digital CMOS design using industry-grade EDA tools.
• To reinforce theoretical concepts through schematic capture, simulation, layout, and post-layout analysis.
• To introduce design practices for parasitic-aware design and layout verification.</td></tr>
<tr><td>Learning Outcomes</td><td colspan="6">By the end of this course, students will be able to:
1. Design and simulate basic digital gates, sequential circuits, and analog building blocks.
2. Create full-custom layouts for analog and digital circuits following design rules.
3. Perform DRC and LVS checks and resolve schematic-layout mismatches.
4. Extract parasitics and analyze their effect on timing and gain in post-layout simulations.
5. Apply layout techniques for matching and symmetry in analog designs.
6. Complete a mini-project integrating schematic, layout, and verification of a CMOS subsystem.</td></tr>
<tr><td>Contents of the course (With approximate break-up of hours for L/T/P)</td><td colspan="6">Tool & Environment Setup: Familiarization with CMOS process PDKs, EDA flow overview (1P)
Digital Schematic Design: Inverter, NAND, NOR, XOR design and simulation 1P
Digital Layout and Post-Layout Analysis: Layout of logic gates, DRC and LVS checks, Floor planning, and placement, Parasitic extraction and delay analysis (1P)
RTL Simulation and Synthesis in HDL: Combinational and sequential logic simulation using Verilog/VHDL (2P)
Clock/Power Routing: Routing, guard rings, metal stack usage, bond pads for I/O (1P)
Schematic Simulation of Analog Blocks: Current mirror, bias circuit, CS amplifier: DC, AC, transient simulation (1P)
Analog Layout and Post-Layout Simulation: Current mirror, differential pair layout, Extracted simulation of analog blocks (1P)
PVT and ESD: for Analog and Digital modules (1P)
Complete ASIC Design from RTL/Schematic to GDS flow with analog/digital blocks standard/custom design 4P (Op-amp, comparators, OTA, biasing networks, ALU, MAC, ADCs, simple ASICs)
Project Review and End Semester Exam: (1P)
Students do one Analog Design and one Digital Design or a Mixed signal design as the project.</td></tr>
</table>

Text Books	1. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 3rd ed., Wiley, 2019. ISBN-13: 978-1-119-45804-1 2. David A. Hodges, Horace G. Jackson & Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, 5th ed., McGraw-Hill Education, 2020. ISBN-13: 978-0-07-802768-0
Reference Books	1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd ed., McGraw-Hill, 2016. ISBN-13: 978-0-07-252493-2 2. Philip E. Allen & Douglas R. Holberg, CMOS Analog Circuit Design, 2nd ed., Oxford University Press, 2002. ISBN-13: 978-0-19-511644-1 3. Eby G. Friedman, Clock Distribution Networks in VLSI Circuits and Systems, Wiley-IEEE Press, 2007. ISBN-13: 978-0-470-12019-2