Modeling of ferroelectric and negative capacitance FDSOI transistors, Part I: Towards RF and Switching applications

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Abstract

In this seminar, an investigation for enhancing the RF Figure-of-Merits (FoM) for FDSOI MOSFET that uses pocket implant in the source/drain regions with ground plane under the influence of back-gate bias, is performed in a well calibrated TCAD simulation tool Silvaco ATLAS. The proposed device architecture shows improvement in effective mobility, subthreshold slope, threshold voltage and off-state current which leads to enhanced the fundamental transconductance term and in turn boosts the linearity. The non-linear behaviour of the proposed FDSOI MOSFET with pockets design is also studied by simulating the DC characteristics and analysing the higher order transconductance coefficients, intermodulation distortion and input intercept point along with the impact of back-gate bias. Further, an investigation on the negative capacitance effect on MFMIS type FDSOI NCFET using two thin-film ferro-dielectric materials, zirconium:HfO_2 (HZO) and silicon:HfO_2(HSO) is performed utilizing the Landau model of ferro-dielectrics for gate-stacking on FDSOI NCFET. The obtained results depict the HZO NCFET offers better performance but lower endurance, while HSO NCFET offers better endurance but slightly lower performance. To further enhance the performance of NCFET the back-gate bias benefit of FDSOI has been investigated. These investigations has shown higher enhancement in performance for both HZO and HSO NCFET(s).

Furthermore, an analytical feasibility and viability of a variant of doped HfO_2 based ferroelectric capacitor i.e. HSO on gate-stack FDSOI for NCFET applications has been investigated. Extensive simulations are carried out to find the optimum ferroelectric thickness of HSO thin-film for the NCFET to operate in hysteresis-free regime. The optimized NCFET is then subjected to the variation of back-gate bias to exploit threshold-voltage shift phenomena to further improve NCFET performance. To extend the investigations towards reliability degradation aspect, the interface trapped charges ($+N_{it}$) are introduced at the oxide-semiconductor interface to observe the reliability deflation caused at process level design and analyze the performance degradation aspect of the NCFET with numerical simulations. Furthermore, the investigations are extended to observe the feasibility of recuperating the degraded performance caused by $+N_{it}$ with utilizing $-V_B$. The performance metrics used in the numerical simulation for the evaluation of HSO ferroelectric NCFET are: sub-threshold slope, charge variation with gate-voltage and ferro voltage, surface potential, V_{TH}, drain-current and amplification factor.