Curriculum and Syllabus for M.Tech.

Electronics and Communication Engineering With Specialization in Microelectronics and VLSI Systems

From The Academic Year 2021

(Approved by Senate-44)

Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram

Chennai-600 127

Semester 1							
S.No	Couse Code	Course Name	Category	L	T	P	C
1	EC5009	MOSFET Modelling for VLSI Circuits	PCC	3	1	0	4
2	EC5010	Analog IC Design	PCC	3	1	0	4
3	EC5011	VLSI Testing and Testable Design	PCC	3	1	0	4
4		Professional Elective Course 1	PEC	3	1	0	4
5		Professional Elective Course 2	PEC	3	1	0	4
6	EC5012	Device Modelling and Simulation Practice	PCC	0	0	3	1.5
7	EC5013	SoPC and VLSI Testing Practice	PCC	0	0	3	1.5
							23.0
Semester 2							
S.No	Course Code	Course Name	Category	L	T	P	C
1	EC5014	Digital IC Design	PCC	3	1	0	4
2	EC5015	VLSI System Design	PCC	3	1	0	4
3	EC5016	VLSI Technology	PCC	3	1	0	4
4		Professional Elective Course 3	PEC	3	1	0	4
5		Professional Elective Course 4	PEC	3	1	0	4
6	EC5017	IC Design Practice#	PCC	0	0	4	2
7	EC5018	High level verification with System Verilog and UVM$	PCC	2	0	4	4
# - As per Senate 50, the credit type was changed from 0 0 3 1.5 to 0 0 4 2 $ - As per Senate 50, the course name was changed to High level verification with System Verilog and UVM (2 0 4 4) from Verification Practice (0 0 3 1.5).							26.0
Semester 3							
S.No	Course Code	Course Name	Category	L	T	P	C
1	EC6003	MT-EC-MVS-Project Phase I (May-July)(Summer Internship)	PCD	0	0	20	10
2	EC6004	MT-EC-MVS-Project Phase II (Aug-Nov)	PCD	0	0	32	16
							26.0
Semester 4							
S.No	Course Code	Course Name	Category	L	T	P	C
1	EC6005	MT-EC-MVS-Project Phase III (Dec-Apr)	PCD	0	0	32	16
							16.0

1. Professional Elective Course is an elective course offered or prescribed by the parent department.
2. 3 Months internship is mandatory, however, the curriculum offers the flexibility to carry out 3-12 Months internship with the approval of the parent department.
3. In line with the guidelines approved by the Senate (Senate 46-07), an M.Tech student can earn a maximum of 6 credits from NPTEL Courses. For all successfully completed NPTEL Courses, the letter grade “H” (Pass) will be awarded and credits of such courses will not be accounted for CGPA calculation.

Semester wise Credit Distribution

Semester						
Category	S1	S2	S3	S4	Total	%
Professional Core Course (PCC)	15	18	0	0	33	34.1
Professional Elective Course (PEC)	8	8	0	0	16	18.2
Professional Career Development (PCD)	0	0	26	16	42	47.7
Total	23.0	26.0	26.0	16.0	91.0	100.0
	23.0	49.0	75.0	91.0		

Course Name	MOSFET Modelling for VLSI Circuits	Course Code	EC5009			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M.Tech	Course Type	Core			
Prerequisite	Basics of Semiconductor Devices, Digital Electronics	Approved In	Senate-44			
Learning Objectives	• To demonstrate and apply basic concepts of semiconductor physics relevant to devices • To describe and use physics-based numerical and analytical device modelling for the inclusion in circuit applications					
Learning Outcomes	At the end of the course, the students would be able to • Model any kind of MOS Devices in 2-D or 3-D • Relate the models for further inclusion in circuits					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Intuitive analysis of MOS Transistor- Two-Terminal MOS Structure – Flatband Voltage, Surface Condition, General Analysis, Inversion, Strong Inversion, Weak Inversion, Small- Signal Capacitance, Three-Terminal MOS Structure (7L+3T) • Long-Channel MOS Transistor, Introduction All-Region Models, Strong Inversion Models, Weak Inversion Models, Source Reference vs. Body Reference, Effective Mobility (5L+2T) • Small-Dimension Effects - Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain-Induced Barrier Lowering, Hot Carrier Effects, Velocity Overshoot Ballistic Operation, Polysilicon Depletion (6L+2L) • Small-Dimension Effects-Modelling for Circuits Simulation- Quantum-Mechanical Effects; Gate Current, Junction Leakage, Scaling and New Technologies, Approaches, and Properties of Good Models, Model Formulation Considerations, Parameter Extraction, Compact Models, Benchmark Tests (7L+3L) • Small-Signal Modelling - Conductance Parameter Definitions and Equivalent Circuits, Conductance Parameters Due to Gate and Body Leakage, Transconductance, Source-Drain and Output Conductance, Capacitance Definitions and Equivalent Circuits, Capacitance Evaluation and Properties, y-Parameter Model, RF Models (11L+2T)					
Essential Reading	1. Y. Tsividis and C. McAndrew, MOSFET modelling for Circuit Simulation, Oxford University Press, 2011					
Supplementary Reading	1. BSIM Manuals available on BSIM homepage on the internet. 2. T. A. Fjeldly, T. Yetterdal and M. Shur, Introduction to Device Modeling and Circuit Simulation, John Wiley, 1998. 3. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 1998. 4. Y. P. Tsividis, Mixed Analog-digital VLSI Devices and Technology, World Scientific Publishing Co Pte Ltd, 2002					

Course Name	Analog IC Design	Course Code	EC5010			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M.Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	• To impart in depth knowledge in CMOS based analog circuits, performance metrics, design and analysis of operational amplifiers and circuits using them • To be capable of designing an opamp for given specifications					
Learning Outcomes	• To analyses effect of mismatch between components in the performance of ICs • To model MOSFET in IC • To analyses noise in different components in the IC • To derive the Data Sheet / Specifications of Single stage, two stage, folded cascade opamps • To understand fully differential operation, opamp and make such circuits					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Components and mismatch in CMOS process, models and Layout techniques. (4L+2T) • MOS Transistor: Layout, model, Body effect, transit frequency. (4L+2T) • Noise: Noise in Resistor, capacitor, and MOSFET, spectral density (4L+2T) • Single stage opamp: Noise, offset, swing limits and slew rate, Loop gain and stability Analysis in two and higher order opamp (10L+2T) • Cascode current mirror, Cascode, Folded Cascode multi stage and Miller compensated op amps. (8L+2T) • Fully differential circuits and opamp, common mode feedback circuits. (6L+2T) • PLL (6L+2T) • Tutorials will include pen-paper analysis and circuit simulation at schematic and layout level					
Essential Reading	1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd edition McGraw-Hill Education, 2016, ISBN: 978-0-07-252493-2					
Supplementary Reading	1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, Analog Integrated Circuit Design, John Wiley & Sons, Inc., 2012, ISBN: 978-0-470-77010-8. 2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th edition, John Wiley & Sons, Inc., 2009. ISBN: 978-0-470-24599-6. 3. Tertulien Ndjountche, CMOS Analog Integrated Circuits High-Speed and Power-Efficient Design, CRC Press Taylor & Francis Group, 2011. ISBN: 978-1-4398- 5500-3.					

Course Name	VLSI Testing and Testable Design	Course Code	EC5011			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M.Tech	Course Type	Core			
Prerequisite	Basics of Digital Electronics	Approved In	Senate-44			
Learning Objectives	• The course aims at imparting skills required for the design of an efficient testable circuit and optimal test vectors to detect all faults					
Learning Outcomes	• At the end of the course, the students would be able to • Model the faults in the combination and sequential circuits • Perform the fault analysis and test pattern generation using ATPG algorithms • Build the testable circuit with test vectors.					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Basic of Test and Role of HDL - Design and Test, Test Concerns, HDLs in Digital System Test, ATE Architecture and Instrumentation. (3L+1T) • Verilog HDL for Design and Test: Using Verilog in Design, Using Verilog in Test, Basic Structures of Verilog, Combinational Circuits, Sequential Circuits, Test bench Techniques. (3L+1T) • Fault and Defect Modelling: Fault Modelling, Structural Gate Level Faults, Issues Related to Gate Level Faults, Fault Collapsing in Verilog. (5L+2T) • Fault Simulation Application and Methods: Fault Simulation, Fault Simulation Applications, Fault Simulation Technologies. (5L+1T) • Test pattern Generation Methods and Algorithm: Test Generation Basics, Controllability and Observability, Random Test Generation. (4L+1T) • Deterministic Test Generation Algorithms: Deterministic Test Generation Methods, Sequential Circuit Test Generation, Test Data Compaction. (4L+1T) • Design for Test by Means of Scan: Making circuits Testable, Testability Insertion, Full Scan DFT Technique, Scan Architectures and RT level Scan Design. (4L+2T) • Standard IEEE Test Access Methods: Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, RT level Boundary Scan and Boundary Scan Description Language. (5L+2T) • Logic Built-in Self-test: BIST Basics, Test Pattern Generation, Output Response Analysis, BIST Architectures, RT Level BIST Design. (4L+1T) • Test Compression: Test Data Compression, Compression Methods and Decompression Methods. (3L+1T) • Memory Testing by Means of Memory BIST: Memory Testing, Memory Structure. (2L+1T)					
Essential Reading	1. ZainalabedinNavabi, Test and Testable Design using HDL Models and Architecture, 1st edition, Springer, 2010, ISBN: 978-1-4419-7547-8.					
Supplementary Reading	1. M. Abramovici, M. A. Breuer and A. D. Figriieta, Digital Systems Testing and Testable Design, Wiley-IEEE Press, 1994, ISBN: 978-0-7803-1062-9. 2. Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, 1st edition, Cambridge University Press, 2003. ISBN: 0521-77356-3 3. Michael L. Bushnell, Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, Springer, 2004. ISBN: 7923-7991-8.					

Course Code	Device Modelling and Simulation Practice	Course Code	EC5012			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	0	0	3	1.5
To be offered for	M.Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	• To make the students familiar with semiconductor device Physics. • To impart a flavour of different semiconductor device modelling with the help of simulation tools. • The lab is intended to teach students about device structure and provide confidence to design the device structure and plotting necessary characteristics in relevant device modelling tools.					
Learning Outcomes	At the end of the course, students would be able to: • simulate and analyse structure, doping profile, terminal characteristics and distributions of carriers, current, field, potential and energy band diagrams within 2-dimensional device structures					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Introduction to Technology computer aided design (TCAD) tools; inputs and outputs of device and process simulations. • Device simulation: observing the terminal characteristics and distributions of carriers, current, field, potential and energy band diagrams within the device. • Process simulation: observation of device structure and doping profile • Simulation of 2-D MOSFETs through device and process simulations • Simulation of novel 3-D transistors such as III-V HEMT, LEDs, FinFETs, GAA devices, solar cells etc, through device simulation • DC, AC, RF mixed mode and noise simulation for the devices					
Essential Reading	1. C K Maiti, "Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications", Jenny Stanford Publishing; 1st Edition, 2017, ISBN: 978-9814745512. 2. Wu, Yung-Chun, Jhan, Yi-Ruei, "3D TCAD Simulation for CMOS Nanoeletronic Devices", Springer, 2017, ISBN 978-981-10-3066-6.					
Supplementary Reading	1. C K Sarkar, "Technology Computer Aided Design: Simulation for VLSI MOSFET", CRC Press, 1st Edition, 2013, ISBN: 978-1466512658. 2. J.-P. Colinge, "FinFETs and Other Multi-Gate Transistors", Springer, 2008, ISBN: 978-0-387-71751-7 3. TCAD Manual (Available Online)					

Course Name	SoPC and VLSI Testing Practice	Course Code	EC5013			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	0	0	3	1.5
To be offered for	M. Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	Design and development complete hardware/software system on FPGA and VLSI testing					
Learning Outcomes	Student can able to design and develop the hardware/software system on FPGA, can able to effectively use commercially available building block (IP) to construct highly integrated systems, can able to efficiently break down complex computational tasks into hardware and software components and build co-processor.					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Verify fault coverage of test patterns, simulate fault, apply test pattern, and observe output • Hands-on on Design for test (DFT) – insert test points, scan chains, to improve testability • Writing ATPG and Designs for Combinational and Sequential Circuits. • Implement BIST for Memory blocks • Scan Chain based Sequential Circuit Testing • Fault Models simulations and verifications, Structural Testing with Fault Models • Implement path delay fault testing • Introduction to System-On-Chip, Register Transfer Language, Folding, Re-timing and Recoding • Protocol and Interface, System-C Components, Basic SoC components, • Electronic system level modelling, Transactional level modelling, Assertion based Design, Network on chip and Bus Structures • SoC Engineering and associated Tools, Architectural design exploration, High Level Design Capture and Synthesis.					
Essential Reading	1. Wang, "VLSI Test Principles and Architectures: Design for Testability", Elsevier; First edition (1 January 2011). ISBN: 9380501552 2. 2. Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, The Zynq Book: Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All, 1st edition, Strathclyde Academic Media, 2014. ISBN: 099297870X.					
Supplementary Reading	1. Wayne Wolf, FPGA based System Design, 1st edition, Prentice Hall, 2004. ISBN: 0131424610. 2. 2. Steve Furber, ARM System on Chip Architecture, 2nd edition, Addison-Wesley, 2000. ISBN: 0201675196.					

Course Name	Digital IC Design	Course Code	EC5014			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	• To impart in depth knowledge in CMOS digital circuits, performance metrics, design procedures for complex combinational and sequential circuits and subsystems. • Students would be able to design and analyse complex digital integrated circuits using semicustom and full custom design procedures.					
Learning Outcomes	• To design series of masks required for IC Design using pen paper up to 5 level and using tool for higher level • To model MOSFETs and Interconnects in ICs • To determine Noise margins, switching voltage, delay parameters, power etc. in ICs • To develop combinational and sequential circuits with static and dynamic CMOS and Pass Transistors • To build arithmetic and Memory ICs					
Course Contents (with approximate breakup of hours for lecture/ tutorial/practice)	• Issues in Digital Integrated Circuit Design (1L) • Fabrication of CMOS IC and packaging (4L+1T) • MOS Device: Threshold Voltage, Secondary Effects, SPICE Models (4L+2T) • Interconnect: Parameters, Electrical Wire Models, SPICE Wire Models (2L+1T) • CMOS Inverter: Transfer Characteristics, Noise margin, Capacitances, Propagation Delay, Power (5L+2T) • Combinational Logic Circuits: Static CMOS, Pass-Transistors, Dynamic CMOS, Dynamic Logic, Cascading (7L+2T) • Sequential Logic Circuits: Timing Metrics, Static and Dynamic Latches, Registers, C2MOS, NORA-CMOS (7L+2T) • Arithmetic Building Blocks: Data paths in Digital Processor Architectures (7L+2T) • Memory and Array Structures: ROM, RAM, CAM, Peripheral Circuitry, PLA and Flash Memory (5L+2T) • Tutorials will include pen-paper analysis and circuit simulation at schematic and layout level					
Essential Reading	1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits, 2nd edition, Pearson, 2003. ISBN-10: 0130909963, ISBN-13: 978-0130909961					
Supplementary Reading	1. John E. Ayers, Digital Integrated Circuits: Analysis and Design, 2 nd edition, CRC Press, 2009. ISBN-10: 142006987X, ISBN-13: 978-1420069877. 2. R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 3rd edition, Wiley-Blackwell, 2010. ISBN-10: 0470881321, ISBN-13: 978-0470881323. 3. Sung-Mo (Steve) Kang, Yusuf Leblebici, Chilwoo Kim, CMOS Digital Integrated Circuits Analysis & Design, 4th edition, McGraw-Hill Higher Education, 2014. ISBN-10: 0073380628, ISBN-13: 978-0073380629.					

Course Name	VLSI System Design	Course Code	EC5015			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M.Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	To impart in depth knowledge in the design, simulation and analyses of complex VLSI circuits including both digital and analog building blocks.					
Learning Outcomes	At the end of the course, students would be able to • Understand circuits and system level issues while integrating sub blocks in integrated circuits • Design and analyze complex VLSI systems using industry level design and verification tools • Gain proficiency in hardware design and scripting languages					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Review of VLSI, Classifications of VLSI Circuits, Design Methodologies and implementation options of VLSI Systems. Y-Chart, Design Abstraction Levels. Modeling Styles (L5+1T) • Designing Fast CMOS Circuits, Various Techniques for Delay Estimation, Logical Effort and Optimization, Low Power Design Techniques, Power Management Techniques at Circuit and System Levels, Tradeoffs in Power & Delay and mitigation Techniques. (L8+T3) • VLSI system design with HDL: Module concepts and modeling styles: Behavioral, dataflow, structural and mixed style modeling, Synthesis and verification of designs. Data path subsystem design: Combinational and sequential circuits, arithmetic circuits and interconnects; implementation of such systems with HDL and design verification including post layout simulations. (L7+T2) • Interconnect Design: Design issues with Resistive, Capacitive and Inductive Parasitic, Interconnect Techniques, Power Distribution and Clock Design: Power Distribution Networks, Clock Generation and Distribution Networks, Layout Designs: Design considerations for signal integrity, manufacturability and reliability. (L7+T2) • Input/output Modules and ESD Protection Networks: Input Buffers, Output Drivers, and ESD Protection Circuits, Overall System Design examples with HDL (L5+T2)					
Essential Reading	Ming-Bo Lin, Introduction to VLSI Systems A logic, circuit and Systems Perspective, CRC Press, 2012, ISBN:978-1-4398-6859.					
Supplementary Reading	1. Neil H. E. Weste, David Money Harris, CMOS VLSI Design, A Circuits and Systems Perspective, 4th edition, Addison-Wesley, Pearson, 2013, ISBN:978-0-321-54774-3. 2. Liming Xiu, VLSI Circuit Design, Methodology Demystified, A conceptual Taxonomy, IEEE Press, A John Wiley & Sons, Inc., 2008, ISBN:978-0-470-12742-1. 3. Hubert Kaeslin, Morgan Kaufman, Top-Down Digital VLSI Design, Elsevier,2015, ISBN: 978-0-12-800730-3.					

Course Name	VLSI Technology	Course Code	EC5016			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	3	1	0	4
To be offered for	M.Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	• To bring both Circuits and System views on technology together. • To offer a profound understanding of the design of complex VLSI devices, and synthesis tools for fabrication.					
Learning Outcomes	At the end of the course, students would be able to • Appreciate the intricacies involved in VLSI circuit fabrication. • Understand the various processes needed to fabricate the VLSI devices. • Learn fabrication steps for existing and coming generation devices.					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Introduction to VLSI Design, Bipolar Junction Transistor Fabrication, MOSFET Fabrication. (L4+T1) • Crystal Structure of Si, Defects in Crystal, Crystal growth (L3+T1) • Epitaxy, Vapour phase Epitaxy, Doping during Epitaxy, Molecular beam Epitaxy (L4+T1) • Oxidation – Kinetics, Rate constants, Dopant Redistribution, Oxide Charges (L5+T2) • Diffusion-Theory of Diffusion, Doping Profiles, Diffusion Systems Ion Implantation - Process, Annealing of Damages, Masking during Implantation (L5+T2) • Lithography, immersion lithography, e-beam lithography (L5+T2) • Etching-Wet Chemical Etching, Dry Etching, Plasma Etching, Si, SiO_2, SiN and other materials (L3+T1) • Deposition-Plasma Deposition, Metallization, Problems in Aluminium Metal contacts, Copper interconnects (L4+T1) • IC BJT - LOCOS, Trench isolation, Poly-emitter-poly-base-BJT and its suitability for high-speed applications (L3+T1) • MOSFET - Metal gate vs. Self-aligned Poly-gate, Tailoring of Device Parameters, CMOS Technology, Latch - up in CMOS, MOSFET structures with strained channels and high-k gate dielectrics, Bi-CMOS Technology (L6+T2))					
Essential Reading	S. K. Ghandhi, VLSI Fabrication Principles- Silicon and Galium Arsenide, John					
Supplementary Reading	1. S. M. Sze, VLSI Technology, Tata McGraw Hill, 2008 2. J. Plummer, M. D. Deal, P. B. Griffin, Silicon VLSI Technology, Fundamentals, Practice and Modelling, Pearson Higher Education, 2000					

Course Name	IC Design Practice#	Course Code	EC5017			
Offered by Department	Electronics and Communication Engineering	Structure (LTPC)	0	0	4	2
To be offered for	M Tech	Course Type	Core			
Prerequisite	NIL	Approved In	Senate-44			
Learning Objectives	• To impart in depth knowledge in the design, simulation and analyses of CMOS based analog integrated circuits especially operational amplifiers and trans conductor amplifiers and Digital integrated circuits. • Students would be able to design and analyse complex analog and digital integrated circuits using industry level analog and digital IC Design tools.					
Learning Outcomes	• To be capable of simulating Schematic level analog circuits with at least 20+ transistors • To be capable of generating layout with full custom / semicustom tools and to perform post layout simulations and extracting parameters to schematic model • To design Digital building blocks using VHDL / Verilog • To generate synthesizable design, create layout and post layout simulations for ASIC Design					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Design of analog ICs with Schematic and layout simulation using Cadence and Synopsys tools (6 weeks) • Design of digital building blocks with Schematic and layout simulation using Cadence and Synopsys tools (6 weeks) • Project will include identifying analog / digital IC from papers of IEEE JSSC, IEEETCASI, IEEE TCASII, IEEE TBioCAS, ISCAS, ISICAS, NEWCAS, APCCAS, MWCAS, simulate both schematic & layout and analyse the results.					
Essential Reading	1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd edition McGraw-Hill Education, 2016, ISBN: 978-0-07-252493-2 2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits, 2nd edition, Pearson, 2003, ISBN-10: 0130909963, ISBN-13: 978-0130909961.					
Supplementary Reading	1. Tony Chan Carusone, David A. Johns, Kenneth W. Martin, Analog Integrated Circuit Design, John Wiley & Sons, Inc., 2012, ISBN: 978-0-470-77010-8. 2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design Of Analog Integrated Circuits, 5th edition, John Wiley & Sons, Inc., 2009. ISBN: 978-0- 470-24599-6 3. Sung-Mo (Steve) Kang, Yusuf Leblebici, Chilwoo Kim, CMOS Digital Integrated Circuits Analysis & Design, 4th edition, Mcgraw-Hill Higher Education, 2014. ISBN-10: 0073380628. 4. Ronald Mehler, Digital Integrated Circuit Design Using Verilog and System Verilog, 1st edition, Newnes, 2015. ISBN: 978-0-12-408059-1.					

Course Name	High level verification with System Verilog and UVM$	Course Code	EC5018			
Offered By Department	Electronics and Communication Engineering	Structure (LTPC)	2	0	4	4
To be offered for	M. Tech	Course Type	Core			
Prerequisite	Hold on Digital Logic Design, and HDL with design flow of VLSI Systems	Approved In	Senate-44			
Learning Objectives	To impart in depth knowledge and hands-on on the Design, Simulation and Verification Flow of Digital Circuits & Systems. Analyses of complex VLSI circuits including both digital and analog building blocks.					
Learning Outcomes	Students would be able to design and analyse complex VLSI systems using industry level Design and verification tools.					
Course Contents (with approximate breakup of hours for lecture/tutorial/ practice)	• Overview of the HDL and Design Methodologies. • Understand and use the System Verilog/HDL RTL design and synthesis features, including new data types, literals, procedural blocks, statements, and operators, relaxation of Verilog language rules, fixes for synthesis issues, enhancements to tasks and functions, new hierarchy and connectivity features, and interfaces, clocking blocks, assertions, cover. Verify the design to ensure 100% coverage. • Generate & analyse functional coverage, code coverage, line coverage & FSM coverage • Basic UVM constructs & classes, design a basic test environment using UVM • System Verilog/HDL verification features, including classes, constrained random stimulus, coverage, strings, queues and dynamic arrays, and learn how to utilize these features for more effective and efficient verification. • Power and Clock Routing, Interconnects design considerations • Floor planning, placement & Routing of the Digital Blocks, physical fixes and signoffs.					
Essential Reading	1. Ming-Bo Lin, Introduction to VLSI Systems A logic, circuit and Systems Perspective, CRC Press, 2012, ISBN:978-1-4398-6859. 2. System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modelling, 2nd Edition, ISBN-13: 978-0387333991					
Supplementary Reading	1. Chris Spear, System Verilog for Verification: A Guide to Learning the Testbench Language Features, Springer. 2012, ISBBN: 978-1461407140. 2. Donald Thomas, Logic Design and Verification Using System Verilog, 2016, ISBN: 1523364025. 3. UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, 2013, ISBN: 0974164933.					