# A Noval SRAM based Packet Classification Architecture

Packet classification is an essential function in modern computer networks that enables the routing and processing of network traffic. To meet the high throughput demands of these networks, hardware architectures for packet classification based on field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) have been developed. This research presents a detailed review of these architectures, including hierarchical classification, parallel processing, and hash-based classification, evaluating the advantages and disadvantages of each approach. The discussion also addresses implementation challenges such as memory management and power consumption, proposing solutions. Finally, the research proposes a comparative analysis of FPGA and ASIC implementations of packet classification, identifying suitable use cases for each approach. These findings provide valuable insights for researchers and practitioners in packet classification and hardware architecture design.

The seminar discuss the effective stride length and the priorityless rule processing for the packet classification architectures.

**(1) Analysys of the Optimal Stride Length:-** Memory requirement and match-line size of a prefix with respect to diffrent length of stride bit is analysed and the optimal length is proposed interms of memory and match-line bit. Compare to all other size of stride bit vector, two-bit stride length gives optimal memory and match-line logic for the prefix match.

**(2) Sedinary Content Addressable Memory (S-CAM):-** Proposing a solution to representing and searching of a sixteen ($Sedinary$) possible state for each two bit stride with respect to four $SRAM$ bits as memory indexing way like Content Addressable Memory.

**(3) Memory Enhanced Sixteen State Prefix Encoding:-** Suggested $S\text{-}CAM$ provides memory optimised prefix encoding with more possible prefix state and reduced match-line bits than conventional $T\,CAM$ . Two-bit stride of a $S\text{-}CAM$ produce exactly same memory as $T\,CAM$ with more possible state and 50% reduction in match-line logic circuit.

**(4) Optimal Range Split Encoding for the proposed S-CAM:-** Recommended range to S-CAM prefix encoding with respect to two-bit stride that uses optimal number of SRAM bits. The range split encoding neither increase the number of rule nor increase the match-line length but increase the number of bits per rule in a linear curve unlike exponential curve as in any literatures.