High Speed Packet Classification Architecture

Abstract: -

Packet classification is a crucial function in modern computer networks for routing and processing network traffic. In order to meet the high throughput requirements of modern networks, packet classification hardware architecture based on field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs) has been developed. The research work presents a detailed review of the packet classification hardware architecture based on FPGA and ASIC. The review covers various approaches, such as hierarchical classification, parallel processing, and hash-based classification, and evaluates the advantages and disadvantages of each approach. The discussion also includes the implementation challenges, including memory management and power consumption, and presents solutions to these challenges. Finally, proposes a comparative analysis of the performance, area, and power consumption of FPGA and ASIC implementations of packet classification, and identifies the suitable use cases for each approach. The findings of the proposed works are expected to provide valuable insights for researchers and practitioners in the field of packet classification and hardware architecture design.

This seminar introduces a novel deterministic approach for implementing a Range Enhanced Reconfigurable Packet Classification Engine (RERPEC) on FPGAs. With the growing demand for high-performance network systems, reconfigurable hardware has emerged as a promising technology for implementing firewalls, routing mechanisms, and new protocols. The proposed framework employs a RAM-based Ternary Match to represent prefix and range prefix, and a rule-reordering technique for priority selection to achieve both best-match and multi-match in a single architecture. The recommended RERPEC architecture offers significant improvements, such as efficient resource utilization, scalability, representation of inverse prefix with a single entry, range expansion with a single rule, and determination of the required FPGA resources for a specific dataset. The proposed design achieves a throughput of up to 520 MPPS with a maximum of 31.3K 104-bit rules using 3.2 Mbits of LUT-RAM-based TCAM. Furthermore, with the integration of BRAM, the complete architecture can support up to 38.5K 104-bit rules while maintaining a throughput of 400 MPPS. Overall, this work provides valuable insights for researchers and practitioners in the field of reconfigurable hardware design and packet classification.