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Synopsis Of

Investigation on Grid Synchronization Techniques of Grid-tied Solar PV System using Pre-Filter based Phase Locked Loop

A Thesis

To be submitted by

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For the award of the degree

Of

DOCTOR OF PHILOSOPHY

1 Abstract

In the current scenario, the integration of renewable energy sources with variable power production into power grids requires a power converter with robust control techniques. In order to formulate the control strategy meticulously, fast and accurate detection of grid phase angle is necessary. Hence, the frequency and phase angle of the grid voltages are vital components to guarantee the synchronization of the grid-connected converter. Additionally, a phase locked loop (PLL) based control algorithm is needed to generate the accurate reference current for the grid-connected converter. PLL is mandatory to track the frequency, and phase angle and filter out the harmonics, interharmonics, and DC offset during distorted grid conditions. This thesis proposes a modified sliding Goertzel discrete Fourier transform (SGDFT) based PLL and an adaptive band-pass filter (ABPF) based PLL to extract the fundamental component during distorted grid conditions. The modified SGDFT based PLL is designed using three degrees of freedom (DOF) of second-order fraction delay using the Lagrange interpolation method to alleviate the integer and noninteger frequency components and strong against several distorted grid conditions, namely, voltage sag, high-frequency harmonics, interharmonics, and dc offset. Furthermore, the proposed PLL precisely extracts the fundamental frequency and phase angle with the faster transient response and attains superior system stability. The detailed mathematical modeling of recommended PLL is analyzed with existing PLLs, such as harmonic, interharmonic, and dc offset PLL (HIHDO PLL), hybrid prefiltering stage PLL (HPFS PLL), and SGDFT-based PLL. Furthermore, ABPF based PLL is proposed in this thesis to estimate the frequency during frequency variation and voltage unbalanced grid conditions. Also, to mitigate the harmonics, interharmonics, and DC offset. To confirm the adaptive nature of the ABPF the gradient algorithm is used to maximize the normalized mean square output and self-adjust the center frequency of the filter during distorted grid conditions. The three-dimensional surface plot can be used to provide the system stability and dynamic response of the filter. For the effectiveness of the proposed study, ABPF is added as a pre-filter to dqCDSC PLL and MAF PLL and a detailed comparative study is made in the paper. In addition to that, the proposed PLL methods are analyzed using a MATLAB®/Simulink environment. Finally, performance is tested experimentally via dSPACE-1104 hardware-in-loop (HIL) simulation.

2 Objectives

In recent years, due to carbon emissions, fossil fuels are not considered a dominant energy source for electricity generation and renewable energy sources (RESs) play a major role in electricity generation. Among all RESs. solar and wind are very popular due to their zero-carbon emission, low maintenance, easy installation, etc. However, they are intermittent in nature and can't be directly connected to the utility grid. Hence, integration with the AC utility grid through grid-connected converters, and the control strategy of the grid-connected converter is important to confirm the stability and reliability of the operation of the utility grid even under abnormal conditions such as grid faults [1]. Appropriate grid synchronization algorithms are required to generate the references currents signals to implement a control strategy on the grid-connected converter and guarantee the output voltage is synchronized well with grid voltages [2]. The grid synchronization methods are predictable to track the precise fundamental frequency and phase of grid voltages/currents in order to produce the reference grid currents accurately. PLL is an imperative tool for achieving grid synchronization and it is required to follow the phase angle, which considerably mitigates the harmonics from distorted grid conditions. The fundamental frequency and phase angle extraction, synchronous reference frame (SRF) PLL has been extensively utilized in grid-connected converters due to its compact structure and simple implementation. Moreover, if three-phase grid voltages are unbalanced or

injected with harmonics, interharmonics, and DC offset component, SRF PLL's bandwidth is diminished which disturb the system stability of the grid-connected converter. In order to overcome the disadvantage of SRF PLL possessing a filtering stage, one way is to use it in control loop (i.e., in-loop filters) of SRF PLL and another is to use it as a pre-filter i.e., before grid voltages. The two important in-loop filters are dq-frame delayed signal cancellation (dqDSC) and moving average filter (MAF) operators. MAF and dqDSC PLLs are recommended to generate positive and negative sequence components [3], [4]. Moreover, single dqDSC cannot alleviate the entire harmonics and interharmonics distortions and hence multiple DSC are added in a parallel manner. However, the parallel DSC causes a stability problem, but a single MAF block of MAF PLL removes harmonic distortions but it does not diminish the interharmonics and DC offset components. HIHDO PLL extracts the phase angle even during abnormalities in grid voltages and high-frequency harmonics injection, despite having the improper dynamic response and high-frequency oscillation during interharmonics conditions due to the harmonics compensation network [5]. HPFS PLL is strong under unbalanced grid voltage conditions in extension to the elimination of even-harmonic components. However, it reveals a slower dynamic response during harmonics and interharmonics conditions [6]. SDFT and sliding Goertzel discrete Fourier transform (SGDFT)-based PLLs are vigorous during harmonics mitigation but require more settling time during dc offset and interharmonics conditions. Adaptive low-pass filter (ALPF) based PLL is presented to remove the component of DC offset. But it may degrade the harmonic filtering capability of the system and requires more settling time and high-frequency overshoot during DC offset and other distorted conditions [7].

Therefore, based on the literature review the objectives of this thesis is,

- To the develop a three-phase adaptive, simple, and powerful grid synchronization tool for grid-tied solar PV system.
- To detect a phase angle of the utility grid and smooth tracking of the phase and frequency with the help of the proposed PLL during abnormal grid conditions.
- For that, a Modified SGDFT & ABPF based PLLs are proposed to precisely extract the fundamental frequency, and phase angle with a faster transient response and attain superior system stability during abnormal grid conditions.
- To analyze the performance of proposed PLL for grid synchronization and comparative study will be made during grid abnormalities such as voltage unbalances, high-frequency harmonics injection, frequency variation, interharmonics, DC offset conditions, etc., and show the efficacy of the proposed PLL.
- A laboratory setup will be developed using the dSPACE-1104 platform and experimental results would be recorded with detailed comparative evaluation in addition to numerical simulations via MATLAB®/Simulink.

3 Existing Gaps Which Were Bridged

Based on the literature review, the following gaps are identified,

There is a need for one adaptive grid synchronization algorithm to extract the fundamental frequency and phase angle for all distorted grid conditions like frequency variation, voltage unbalance, harmonics, inter harmonic and dc-offset injection. In addition, there is a need to inject power into the grid, with low Total Harmonic distortion (THD) of the current. However, any distorted grid conditions do not degrade the dynamic performance of the algorithm.

The above research gaps are bridged in this thesis

(a) Modified SGDFT based PLL is designed using three degrees of freedom (DOF) of second-order fraction delay using the Lagrange interpolation method to alleviate the harmonics, interharmonics and DC offset components and robust against several distorted grid conditions, namely, voltage sag, high-frequency harmonics, interharmonics, and dc offset. Furthermore, the proposed PLL precisely extracts the fundamental frequency and phase angle with less settling time and reduces the THD as per IEEE 519-2014 standards.

(b) A novel ABPF based PLL is proposed specifically for grid frequency variation conditions and unbalanced voltage conditions. To guarantee the adaptive nature of the bandpass filter, the mean square output is maximized, and the center frequency is auto-adjusted using a gradient algorithm for various distorted grid voltage conditions. The three-dimensional surface plot is provided to confirm the stability region of the filter. Furthermore, ABPF prefilter-based dqCDSC PLL and MAF PLL are adequate for harmonics, interharmonics and DC offset mitigation with less settling time and reduced THD as per IEEE 519-2014 standards during frequency variation, unbalanced voltage and other distorted grid conditions.

4 Most Important Contributions

4.1 Accurate phase detection system using modified SGDFT-based PLL for three-phase grid-interactive power converter during interharmonic conditions

The primary contributions of this chapter are as follows:

(a) Modified sliding Goertzel discrete Fourier transform (SGDFT) based PLL has been proposed to extract the fundamental frequency and phase angle with the faster transient response during distorted grid conditions.

(b) The comb filter of the modified SGDFT based PLL is designed using three degrees of freedom (DOF) of second-order fraction delay using the Lagrange interpolation method to alleviate the noninteger frequency components.

(c) Stability of the modified SGDFT based PLL can be concluded using a three-dimensional (3-D) surface plot.

(d) The detailed mathematical modeling and frequency response of the proposed PLL is analyzed with existing PLLs, such as harmonic, interharmonic, and dc offset PLL (HIHDO PLL), hybrid prefiltering stage PLL (HPFS PLL), and SGDFT-based PLL.

(e) The numerical simulations for the proposed PLL are carried out using MATLAB®/Simulink environment and the performance of the recommended PLL is tested experimentally through the dSPACE 1104 DSP platform.

The general structure of the modified SGDFT filter is shown in Fig. 1. If noninteger frequency components are present in the three-phase grid voltages, then SGDFT-based PLL is inadequate for extracting the fundamental frequency components due to the single DOF structure of the comb filter. Therefore, Fig. 2. Illustrate the three DOFs are introduced in the comb filter of modified SGDFT using the Lagrange interpolation method for alleviating the noninteger frequency components. Hence, the modified SGDFT-based PLL is adequate to extricate the fundamental frequency and phase angle components during the interharmonic condition.

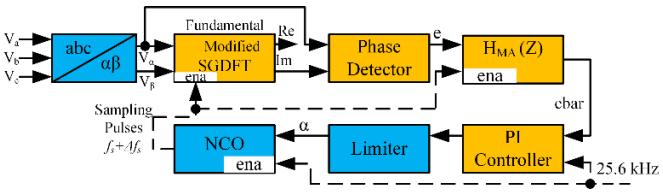

Fig. 1 Block diagram of modified SGDFT based PLL

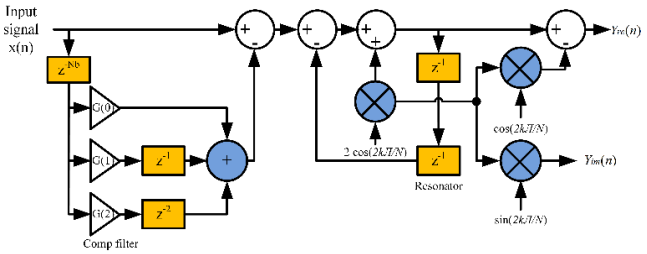

Fig. 2. General structure of modified SGDFT filter.

Fig. 3. shows the frequency response of fraction delay using the Lagrange interpolation method at a different order of the filter and different "*D*" values. For validation, "*D*" can be selected as 0.2 (red line), 0.5 (green line), and 0.9 (blue line). The magnitude of fraction delay in the third-order n = 3 (dotted line) exceeds the unit amplitude, which may propose a stability problem. However, the third-order fraction delay required more multiplication and addition operations than the second-order fraction delay. Therefore, the second-order fraction delay is introduced to the Lagrange interpolation method.

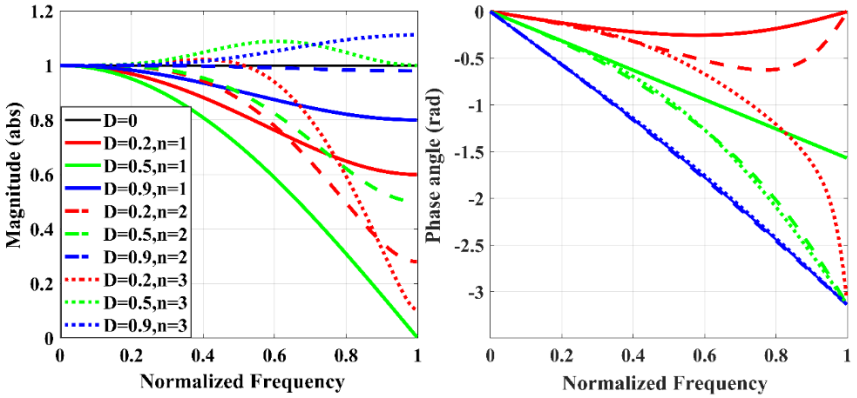

Fig. 3. Frequency response (magnitude and phase angle) of fraction delay using the Lagrange interpolation method.

The output of MAF filter is enforced to the PI controller for obtaining the steady-state value. Accordingly, the PI controller is tuned using the symmetrical optimization (SO) method, which further transferred to the limiter to obtain a steady state (or dc) value (α) the NCO. The fixed sampling pulses are generated by the NCO at an appropriate sampling rate. Fig. 4. shows the gain impact of the PI controller, which states the stability of the proposed PLL. The 3-D surface plot concludes the modified SGDFT-based PLL, which states that the design of the PI controller must consider ω_f/ω ratio (ω_f = [0.5,5]* ω) and should be designed higher than that value. Moreover, it impacts the design parameters, i.e., the plot indicates the sensitivity of k_i (if compared to k_p) toward the destabilization.

The transfer function for the real and imaginary part of modified SGDFT is expressed in (1) respectively. From the frequency response of Fig. 5 (Redline), it is concluded that the modified SGDFT filter has better filtering capability and can completely alleviate interharmonic components including harmonic and DC offset. Moreover, characteristics of the modified SGDFT filter neither act as a passband nor as a stopband filter.

$$[H_{\mathrm{Re}}(z)] = \frac{\left(1 - e^{j\left(\frac{2\pi k}{N}\right)} z^{-1}\right)\left(1 - \sum_{K=0}^{n} G(K) z^{-(K+N_b)}\right)}{\left(1 - 2\cos(2\pi k/N) z^{-1} + z^{-2}\right)} \tag{1}$$

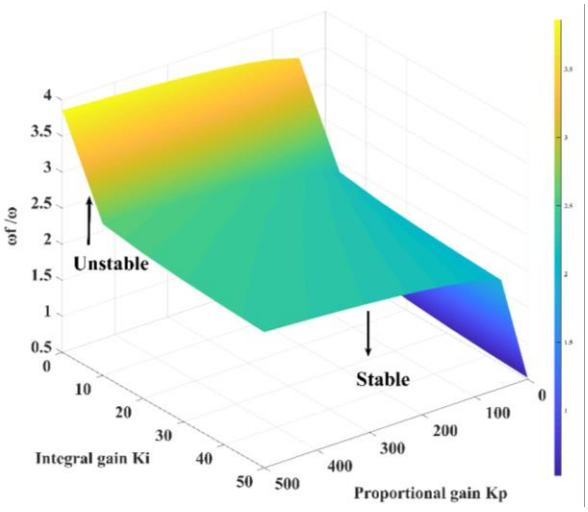

Fig. 4. Impact of PI controller gain on stability.

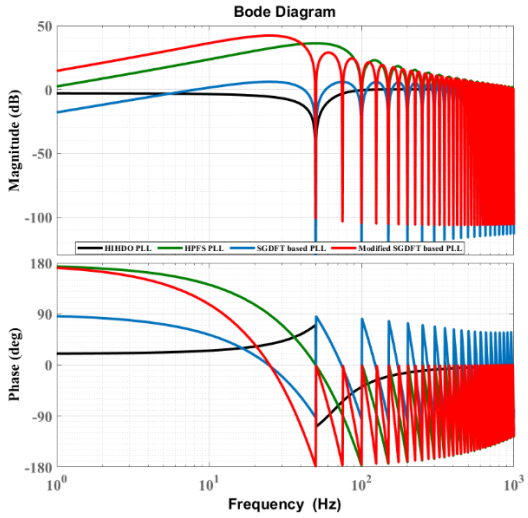

Fig. 5. Frequency response of different PLLs

Simulation and experimental results discussion during interharmonics condition

The performance of the proposed modified SGDFT-based PLL is evaluated and tested by the MATLAB®/Simulink toolbox, and results are compared with existing PLL during voltage sag, high-frequency harmonics, interharmonics, and DC offset grid conditions. For this simulation and experimental studies, the following parameters are adopted: three-phase input voltage (V_{in}) = 415 V (line-to-line rms) amplitude normalized to 1-p.u. input frequency *f* = 50 Hz and sampling frequency *fs* = 6400 Hz.

In order to validate the proposed PLL technique, experiments results are analyzed in this chapter using DSP based dSPACE DS-1104 dSPACE platform. However, it includes several I/O (input/output) using a CLP-1104 board and several analog to digital converter (ADC) and digital to analog converter (DAC). The three-phase signal originates from a DS1104 ADC board whose input is an analog three-phase simulated voltage. All the experimental waveforms below are captured from 4 channel Keysight digital storage oscilloscope (DSO) DSOX2024A, and the hardware-in loop simulation (HIL) setup is depicted in Fig. 6. The experimental setup of the grid-tied solar PV system is adopted for validation of the proposed PLL as illustrated in Fig. 7. The advantages of the proposed modified SGDFT based PLL are analyzed in this chapter using the experimental results.

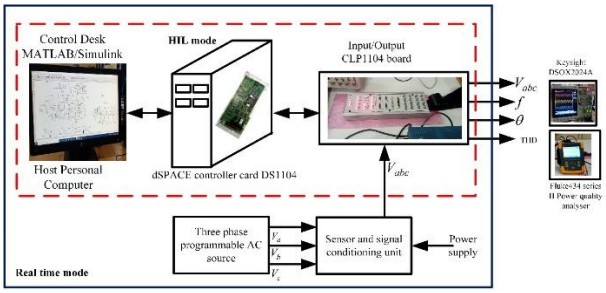

Fig. 6. Hardware-in loop (HIL) set up for grid-tied solar PV system

Fig. 7. Overall experimental setup of grid-tied solar PV system

The three-phase grid voltages (V_{abc} = 1p.u.*)* are distorted with 4% of 7.5th interharmonics and 8% of 5.5th interharmonics, and these voltages are applied to different PLLs using MATLAB®/Simulink toolbox. The modified SGDFT-based PLL is invulnerable to interharmonics grid conditions because three DOFs of fraction delay are connected along with the comb filter of SGDFT, which removes the noninteger frequency components from the grid. In addition to that, the fundamental frequency

extracted by the proposed PLL is within 0.05 grid cycle and with 0.2 Hz frequency overshoot. Instead of this, the HIHDO PLL and HPFS PLL have undesired oscillations while estimating the phase error and frequency. The three-phase balanced voltage is applied until 0.4 s. However, at 0.4 s, the three-phase grid voltage encloses the 50-Hz fundamental frequency with a voltage of 1 p. u. with 8% of 5.5th of interharmonic and 4% of 7.5th interharmonics till 0.5 s. Again, from 0.5 to 0.6 s, a normal balanced three-phase voltage is applied, which is shown in Fig. 8.

The interharmonics three-phase voltages are enforced to different PLL in the experimental results are illustrated in Fig. 9(a). The HIHDO PLL and HPFS PLL show a sluggish dynamic response and higher frequency oscillation as depicted in Fig. 9(b) However, the proposed PLL has a better ability to track the fundamental frequency, i.e., 12 ms, without involving any steady-state oscillation, as shown in Fig. 9(c). In addition, the proposed PLL has a good ability to provide the ripple-free phase angle estimation, is shown in Fig. 9(c). The THD of the interharmonics contaminated grid voltages is 24.86%, and the THD of fundamental grid voltages extracted by modified SGDFT-based PLL is reduced to 2.3%, as shown in Fig. 9(d). Thus, the modified SGDFT-based PLL can extract the fundamental frequency component and alleviate noninteger frequency components with a fast-dynamic response.

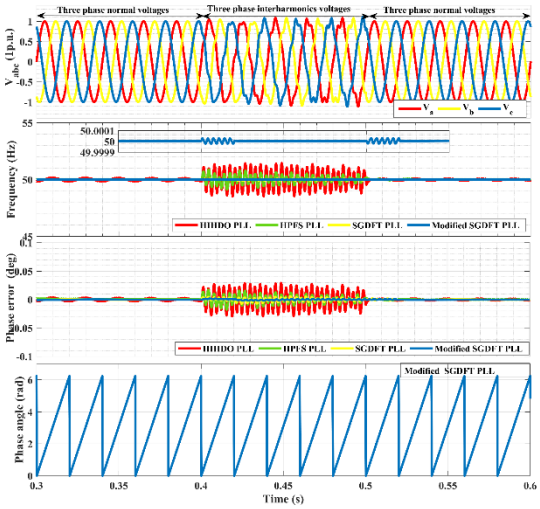

Fig. 8. Simulation response of the PLLs under interharmonics condition.

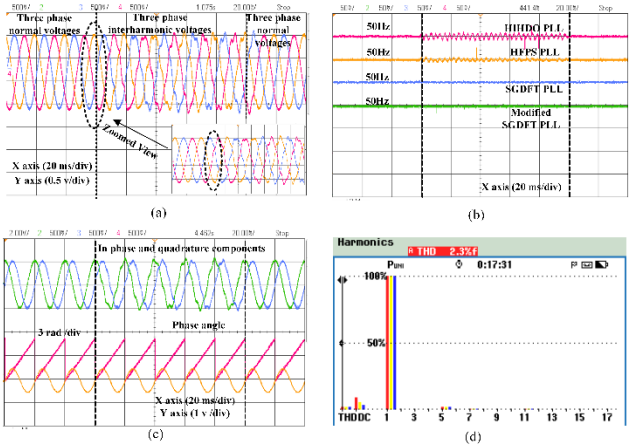

Fig. 9. Experimental results during interharmonics with HIL Simulation

4.2 A novel adaptive band-pass filter based PLL for grid synchronization under distorted grid conditions

The primary contributions of this chapter are as follows:

(a) A novel adaptive band-pass filter (ABPF) has been proposed and can be added as a pre-filter of PLL structures without modifying design of the PLL.

(b) To confirm the adaptive nature of the ABPF the gradient algorithm is used to maximize the normalized mean square output and self-adjust the center frequency of the filter during distorted grid conditions.

(c) The three-dimensional surface plot can be used to provide the system stability and dynamic response of the filter. For the effectiveness of the proposed study, ABPF is added as a pre-filter to dqCDSC PLL and MAF PLL and a detailed comparative study is made in the thesis.

(d) In addition to that, the proposed ABPF based dqCDSC PLL and ABPF based MAF PLL methods are analyzed using MATLAB®/Simulink environment. Finally, performance is tested in real time via dSPACE-1104 hardware-in-loop (HIL) simulation.

The block diagram of the proposed ABPF based PLL is represented in Fig. 10 and it contains pre-filters and an in-loop filter. MAF or dqCDSC operators act as an in-loop filter. Indeed, MAF and dqCDSC PLL yield good performance in terms of frequency variation conditions, but only if the frequency is close to the nominal value. Nevertheless, their performance is inferior when the grid frequencies vary from the nominal value. In order to mitigate this problem, the ABPF is used as a pre-filter to extract the fundamental frequency component from three-phase voltages under any abnormal grid conditions. If DC offset is inserted into any PLL technique the bandwidth of the filter may change, but ABPF can be an add-on to all PLL techniques so that the bandwidth of the filter does not change.

Laplace transform of band-pass filter (BPF) is given in (2)

$$BPF(s) = \frac{s\omega_c k}{s^2 + ks\omega_c + \omega_c^2} \tag{2}$$

Where, ω_c is the cut-off frequency of BPF, now assume that ω_c of the BPF is selected by considering the functionality at the nominal frequency ω_{fn} which can be made adaptive i.e., $\omega_c(\omega_f / \omega_{fn})$. However, the range of ω_c is dependent upon the ω_e and ω_{fn} .The continuous-time of BPF can be written in discrete domain using bilinear transform therefore the discrete domain BPF is obtained and is expressed in (3).

$$BPF(z) = \frac{2\omega_c\left(1-z^{-2}\right)k}{4\left(1-z^{-1}\right)^2 + 2k\omega_c T_s\left(1-z^{-2}\right) + \omega_c^2 T_s^2\left(1+z^{-1}\right)^2} \tag{3}$$

The value of the damping factor ('k') determines the bandwidth of BPF. For accurate filter response, the value 'k' considers being low. By using (3) the discrete implementation of ABPF is depicted in Fig. 11.

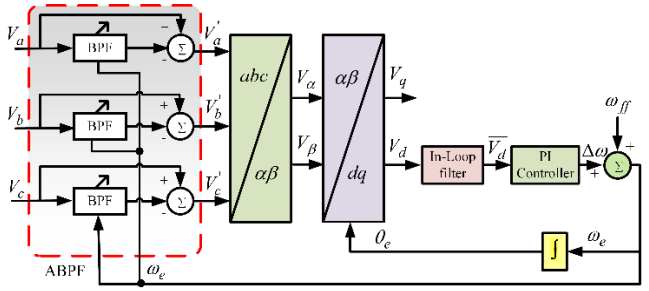

Fig. 10. Block diagram of proposed ABPF based PLL

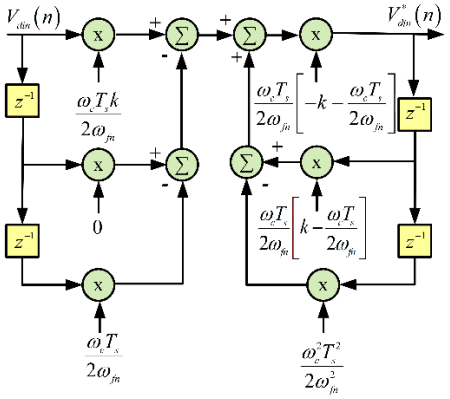

Fig. 11. Discrete Implementation of ABPF

Bode plot of BPF is depicted in Fig. 12 for different values of 'k', here ω=2*л*50 rad/sec. Equation (2) is used to obtain the bode plot which acts as a pre-filter in the proposed system. At fundamental frequency (50 Hz), pre-filter magnitude and phase angle is 0 dB and 0 deg respectively.

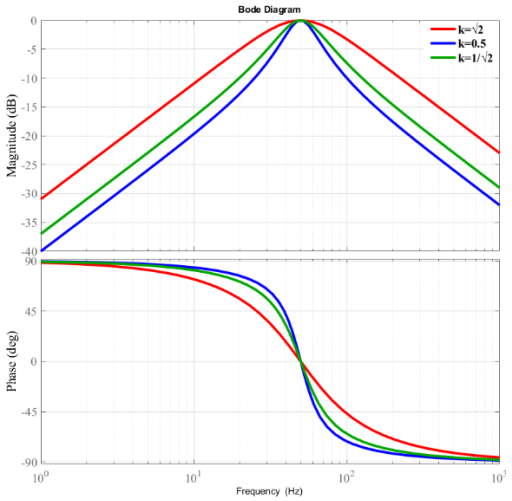

Fig. 12. Bode plot of ABPF with different values of k

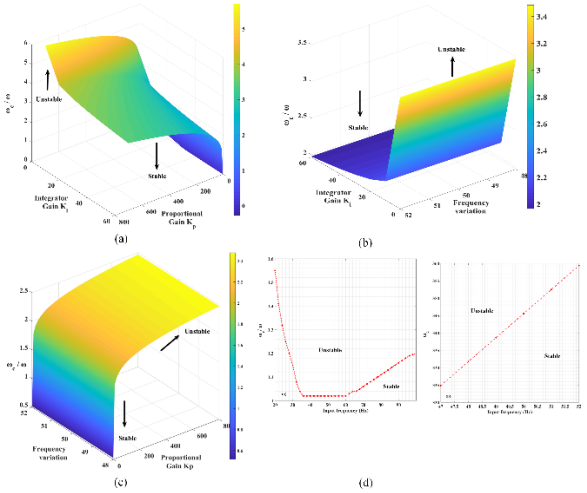

Fig. 13. Regions of stability of ABPF based PLL.

The frequency variation and voltage unbalanced are external inputs to PLL and impact PLL's dynamic performance and stability margins [8]. The ABPF based PLL design parameters of PI gains (k_p and k_i) and cut-off frequency (ω_c) are considered stability boundaries of ABPF based PLL. Increasing bandwidth, the ω_c used in ABPF based PLL supremacy to instability. But, decreasing the ω_c leads to a slow dynamic response. Therefore, the range of ω_c is bounded by a lower performance limit and upper stability limit. The three-dimensional (3-D), surface plots are used to validate the stability region as depicted in Fig. 13.

The balanced three-phase grid voltage is applied with the fundamental frequency of 50 Hz from time (t) = 0.3 s to 0.4 s. However, at t = 0.4 s, the frequency changes from 50 Hz to 51 Hz and persists until t=0.7 s. These frequency variation three-phase voltages are applied to different PLLs using the MATLAB®/Simulink toolbox is depicted in Fig. 14.The proposed PLL provides a faster frequency estimation with reduced frequency and phase overshoot as compared to ALPF based PLL because a gradient algorithm is used to build adaptive BPF and fix the constant cut-off frequency during frequency variation conditions. The frequency variation three-phase voltages are enforced to different PLL in the experimental results are illustrated in Fig. 15(a). Proposed ABPF based dqCDSC and ABPF based MAF PLLs are able to track the grid frequency with a low-frequency overshoot of 12 Hz and less settling time of 42 ms (2.1 cycles) & 38 ms (1.9 cycles) respectively are illustrated in Fig. 15(b) and Fig. 15(c). In addition to that, the proposed PLLs are precisely extracting the in-phase and quadrature components without any distortion is shown in Fig. 15(d).

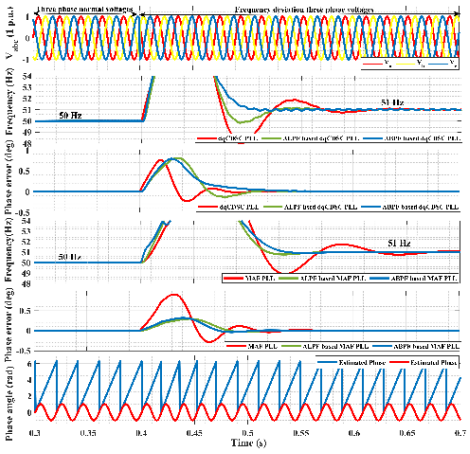

Fig. 14. Simulation results during frequency variation in grid voltages

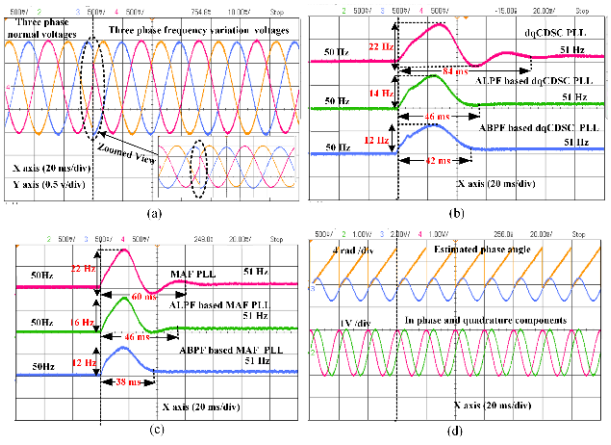

Fig. 15. Experimental responses during frequency variation with HIL simulation

5 Conclusions

Grid synchronization algorithms are significant in the control of GSC, for estimating the fundamental frequency and implementing stable control strategies under distorted grid conditions. PLL is an integral part of grid synchronization, in which perfect performance of PLL is mandatory to obtain a fast steady-state response and dynamic response. This thesis proposed modified SGDFT based PLL and ABPF based PLL to extract the fundamental frequency, and phase angle with a faster transient response and attains superior system stability, and mitigate harmonics, interharmonics, and DC offset components. The comb filter of modified SGDFT-based PLL, which is designed using the three DOFs of second-order fraction delay using the Lagrange interpolation method to alleviate the noninteger frequency components. The modified SGDFT-based PLL was proposed at the constant sampling frequency, indeed to extract the fundamental frequency, amplitude, and phase angle for good synchronization. Simultaneously, negligible harmonics component, dc offset component, and settling time show the adequacy of the proposed work. ABPF based PLL is proposed specifically for grid frequency variation conditions. To guarantee the adaptive nature of the bandpass filter, the mean square output is maximized, and the center frequency is auto-adjusted using a gradient algorithm for various distorted grid voltage conditions. The three-dimensional surface plot is provided to confirm the stability region of the filter. The validation of Modified SGDFT based PLL and ABPF based PLL are demonstrated by MATLAB®/Simulink environment followed by the experimental evaluation using the dSPACE-1104 controller. From the study, it is concluded that the proposed PLLs are adequate for harmonics, interharmonics and DC offset mitigation with less settling time and reduced THD as per IEEE 519-2014 standards. Likewise, the proposed PLLs provide improved stability and fast dynamic response. In addition, the modified SGDFT-based PLL synchronization technique is compared with HIHDO PLL, HPFS PLL, and SGDFT-based PLL during voltage sag, high-frequency harmonic injection, interharmonic injection, and DC offset conditions to manifest the enhancement among the state-of-the-art PLL synchronization techniques. Concurrently, the proposed ABPF based dqCDSC PLL and ABPF based MAF PLL techniques are compared with ALPF based dqCDSC PLL, ALPF based MAF PLL, dqCDSC PLL, and MAF PLL during frequency variation, harmonics injection, interharmonics, DC offset, and unbalanced grid conditions. Furthermore, the recommended PLLs will utilize grid monitoring, processing, and measuring during distorted grid conditions. These proposed PLLs will also be validated during grid fault conditions for detection of phase angle to implement the control strategy using a grid-connected power converter for ensuring the safe operation of the grid-tied solar PV system.

6 Organization of the Thesis

The proposed outline of the thesis is as follows:

(a) Chapter 1: Introduction

(b) Chapter 2: Phase locked loop (PLL) for grid synchronization.

(c) Chapter 3: A Modified SGDFT-based PLL for grid synchronization during interharmonic conditions

(d) Chapter 4: A novel adaptive band-pass filter based PLL for grid synchronization under distorted grid conditions.

(e) Chapter 5: Conclusions and future scope

7 List of Publications

Papers in Refereed Journals

(a) **Sridharan. K**, B.Chitti Babu, "Accurate Phase Detection System using Modified SGDFT based PLL for Three-phase Grid-interactive Power Converter during Interharmonic Conditions", *IEEE Trans. On Instrumentation and Measurement*, (I.F: 4), Vol. 71, Pp. 1-11, 2022, Art no. 9000311, Feb 2022.

(b) **Sridharan. K**, B. Chitti Babu, "A Novel Adaptive Band-Pass Filter Based PLL for Grid Synchronization under Distorted Grid Conditions", *IEEE Trans. On Instrumentation and Measurement*, (I.F: 4) March 2022 - Accepted.

(c) Subham Ku.Jalan **,** B. Chitti Babu, **Sridharan. K** and Gayadhar Panda " A Novel Phase Locked Loop based Control Strategy for a Three-phase Grid-tied Solar PV System,", *IEEE Trans. On Industry Applications* (Man. ID: 2022-IACC-0248)- Under Review.

Presentation in Conference

(a) **Sridharan. K** and B. Chitti Babu, "An Improved Grid Synchronization Method of Grid-Interactive Power Converter System During Distorted Grid Conditions," In Proc. 2020 IEEE 9th Power India International Conference (PIICON), pp.1-6, Sonipat, India, March 2020.

Key References

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