INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, DESIGN AND MANUFACTURING, (IIITDM) KANCHEEPURAM

SPARC Sponsored Workshop on Software Hardware Co-Design (SPARC-SwHwCoD)

17–23 December 2025 | Hybrid Mode (In-Person + Online)



IIITDM KANCHEEPURAM, an Institute of National Importance under the Ministry of Education, specializes in IT, Design, and Manufacturing-focused engineering education and research. With strong industry linkages and state-of-the-art laboratories, the 51-acre Chennai campus offers an excellent environment for learning, research, and innovation.

The Department of Electronics and Communication Engineering is a leading centre for research in VLSI & Embedded Systems, Neuromorphic Computing, RF and Microwave Systems, Signal Processing, and Communication Systems. It hosts major sponsored projects from MoE, DST and ANRF, MeitY, ICMR, DRDO, and industry, supported by modern laboratories for UG, PG, and PhD programmes.

The Scheme for Promotion of Academic and Research Collaboration (SPARC) is an MoE initiative that promotes joint research initiatives between Indian and international institutions, supporting workshops, and faculty and student exchanges to foster high-impact collaboration.

Project Title: *NVM-based In-Memory Computing to Accelerate Neuromorphic Design for ECG/EEG Data Analysis*
Indian PI : Dr. Binsu J. Kailath, Professor, IIITDM Kancheepuram
Indian Co-PI : Dr. S. Kalpana, IIITDM Kancheepuram
International PI : Prof. Yu Cao, University of Minnesota, USA
International Co-PI : Dr. R.V. Joshi, IBM T.J.W.R.C., USA

Workshop Overview: What Participants Will Learn

This workshop introduces participants to the foundations and emerging practices of software–hardware co-design, a critical paradigm for modern edge-AI, heterogeneous computing, and accelerator-driven systems. Through expert lectures, participants will explore FPGA-specific logic design, architecture–algorithm co-optimization, hardware–software partitioning strategies, and design methodologies used in industry for AI/ML acceleration. The sessions emphasize how architectural choices, tool flows, and algorithmic constraints interact, enabling participants to understand how high-level models translate into efficient hardware implementations.

In the afternoon, hands-on lab sessions will guide participants through the complete VLSI/ASIC design flow—from RTL design and verification to synthesis, physical design, and tape-out preparation. Conducted by IIITDM scholars and an industry expert, the labs focus on practical usage, debugging, and sign-off steps.

Together, the talks and labs provide a balanced mix of theory and practical skills for modern hardware development.

In-Person seats limited to 50

📌 Senate Hall, Admin Block, IIITDM Kancheepuram

Register Now!! Closes by 15th Dec!!!

This workshop brings together leading experts in architecture algorithm co-design, FPGA/ASIC implementation, accelerator design for AI/ML workloads, and modern tool flows that unify software and hardware optimization.

Patron
Prof. M.V. Kartikeyan Director

Co-Patron
Dr. B. Chitti Babu, Head of the Department

Organizers
Prof. Binsu J. Kailath & Dr. S. Kalpana, Department of ECE

Invited Speakers:
- Prof. Yu Cao, University of Minnesota
- Dr. R. V. Joshi, IBM T. J. W. Research Center
- Dr. Ayan Palchaudhuri, IIT Bhuvaneswar
- Dr. Binod Kumar, IIT Jodhpur
- Dr. Devashree Tripathy, IIT Bhuvaneswar
- Dr. Sateesh, Industry Expert
- Dr. Anand Mukhopadhyay, MathWorks
- Mr. Pradeep Gautam, DRDO
- Mr. Shankar, Industry Expert
- Mr. Bharathwaj T. A, eInfochips Chennai

Key Highlights:
Expert Lecture Sessions Including
- Fundamentals of Software–Hardware Co-Design
- FPGA-Specific Logic Design & Optimization
- HW–SW Partitioning for AI/ML Workloads
- Accelerator Architectures for Edge/Embedded AI
- System-Level Co-Optimn for Perf., Power & Area
- Chip–Package–System Co-Design Perspectives

Hands-on VLSI/ASIC Design Labs
- Complete VLSI/ASIC Design Flow
- RTL Design & Functional Verification
- Logic Synthesis & Physical Design
- Tape-Out Preparation & Real-World Practices

Organizing Committee:
Priya K - 9599666075, Asha V - 7676489812, Vasanthi R - 7708474072, Divya Mohan M - 8921211926