

SPARC Sponsored Workshop on In-Memory Computing (SPARC-IMC)

10-16 December 2025 | Hybrid Mode (In-Person + Online)

This workshop brings together leading experts in **RRAM/PCM-based IMC**, **memristive logic**, **neuromorphic circuits**, **PIM architectures**, and **low-power computing** for next-generation intelligent systems.

Patron

Prof. M.V. Kartikeyan Director

Co-Patron

Dr. B. Chitti Babu, Head of the Department

Organizers

Prof. Binsu J. Kailath & Dr. S. Kalpana,

Department of ECE

Invited Speakers:

- **Prof. Yu Cao**, University of Minnesota
- **Dr. R. V. Joshi**, IBM T. J. W. Research Center
- **Dr. Brajesh Rawat**, IIT Ropar
- **Dr. Bhupendra S. Reniwal**, IIT Jodhpur
- **Prof. Santosh K. Vishvakarma**, IIT Indore
- **Dr. Tanmay Dutta**, IIT Guwahati
- **Dr. Sandip Lashkare**, IIT Gandhinagar
- **Dr. Avinash Lahgere**, IIT Kanpur
- **Dr. Vikramkumar Pudi**, IIT Tirupati
- **Dr. Shubham Sahay**, IIT Kanpur
- **Mr. Bharathwaj T. A.**, eInfochips Chennai

Key Highlights:

Expert Lecture Sessions Including

- **Fundamentals of In-Memory Computing (IMC)**
- **Memristor & NVM-Based Computing**
- **Device Reliability & Scaling Challenges**
- **Hybrid Architectures for AI Acceleration**

Hands-on VLSI/ASIC Design Labs

- **Complete VLSI/ASIC Design Flow**
- **RTL Design & Functional Verification**
- **Logic Synthesis & Physical Design**
- **Tape-Out Preparation & Real-World Practices**

Organizing Committee:

- **Priya K**, 9599666075
- **Asha V**, 7676489812
- **Sushmi R**, 8838961362
- **Vasanthi R**, 7708474072
- **Divya Mohan M**, 8921211926

IIITDM KANCHEEPURAM, an **Institute of National Importance** under the Ministry of Education, specializes in **IT, Design, and Manufacturing-focused engineering education and research**. With strong industry linkages and state-of-the-art laboratories, the 51-acre Chennai campus offers an excellent environment for learning, research, and innovation.

The Department of Electronics and Communication Engineering is a leading centre for research in **VLSI & Embedded Systems, Neuromorphic Computing, RF and Microwave Systems, Signal Processing, and Communication Systems**. It hosts major sponsored projects from **MoE, DST and ANRF, MeitY, ICMR, DRDO, and industry**, supported by modern laboratories for **UG, PG, and PhD programmes**.

The Scheme for Promotion of Academic and Research Collaboration (SPARC) is an MoE initiative that promotes joint research initiatives between Indian and international institutions, supporting workshops, and faculty and student exchanges to foster high-impact collaboration.

Project Title: *NVM-based In-Memory Computing to Accelerate Neuromorphic Design for ECG/EEG Data Analysis*

Indian PI : Dr. Binsu J. Kailath, Professor, IIITDM Kancheepuram

Indian Co-PI : Dr. S. Kalpana, IIITDM Kancheepuram

International PI : Prof. Yu Cao, University of Minnesota, USA

International Co-PI : Dr. R.V. Joshi, IBM T.J.W.R.C., USA

Workshop Overview: What Participants Will Learn

The forenoon sessions feature expert lectures covering key themes in **In-Memory Computing (IMC)**, including memristor-based architectures, device-level limitations of NVMs, reliability challenges, and hybrid CMOS–NVM computing approaches. These talks provide a strong conceptual foundation, highlight recent research trends, and showcase practical insights from ongoing global work.

In the afternoon, hands-on lab sessions will take participants through a **complete VLSI/ASIC design flow**—from architecture definition and RTL development to verification, synthesis, physical design, and tape-out preparation. Led by IIITDM scholars and an industry expert, these sessions emphasize practical tool usage, debugging, and sign-off practices.

Together, the lectures and labs offer a holistic blend of **theory and practical design experience**, preparing participants to engage confidently with modern hardware development.

In-Person seats limited to 50

★ Senate Hall, Admin Block
IIITDM Kancheepuram, Chennai.

**Limited
Seats
Available
Register
Now**

